PATENT

Atty Docket No.: 10004808-1
Appl. Ser. No.: 09/891,324

IN THE CLAIMS:

Please find below a listing of all of the pending claims. The statuses of the claims are set forth in parentheses.

1. (Previously presented) A method of forming a by-pass capacitor on a multi-level metallization device, said method comprising:

forming a first electrode in a first dielectric layer of said multi-level metallization device;

depositing a substantially thin insulator layer over said first dielectric layer of said multi-level metallization device; and

forming a second electrode in a second dielectric layer, wherein said second dielectric layer is formed over said substantially thin insulator layer.

2. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, said method further comprising:

patterning said substantially thin insulator layer to substantially cover said first electrode; and

adjusting a thickness of said substantially thin insulator layer.

3. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 2, wherein a dielectric constant of said substantially thin insulator layer is substantially high.

4. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said substantially thin insulator layer includes silicon nitride.

5. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said thickness of said substantially thin insulator layer is between 50 and 100 angstroms.

6. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said dielectric constant of said substantially thin insulator layer is between 4 and 100.

7. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, said method further comprising:

depositing the second dielectric layer over said substantially thin insulator layer; and

etching at least one via, said at least one via adapted to receive said second electrode.

8. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 7, said method further comprising:

polishing said second electrode.

9. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, wherein said forming said first electrode comprises:

etching said first electrode in the first dielectric layer of said multi-level metallization device.

10. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, further comprising:

forming the first electrode in a parallel line configuration.

11. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, further comprising:

forming the second electrode in a parallel line configuration.

12. (Previously presented) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, wherein said substantially thin insulator layer comprises a composite of materials.

13. (Original) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 12, wherein said composite of materials includes PZT and platinum.